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EXAMINER	
NGUYEN, TANH Q	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/592,009	LEE ET AL.	
	Examiner	Art Unit	
	Tanh Q. Nguyen	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 May 2007 (RCE)*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 December 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☒ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *05/14/07*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on April 25, 2007 has been entered.

Oath/Declaration

2. The oath or declaration is defective. A new oath or declaration in compliance with 37 CFR 1.67(a) identifying this application, by application number and filing date is required. See MPEP §§ 602.01 and 602.02.

The oath or declaration is defective because it does not identify the mailing address of each inventor. A mailing address is an address at which an inventor customarily receives his or her mail and may be either a home or business address. The mailing address should include the ZIP Code designation. The mailing address may be provided in an application data sheet or a supplemental oath or declaration. See 37 CFR 1.63(c) and 37 CFR 1.76.

Information Disclosure Statement

3. The information disclosure statement filed May 14, 2007 includes NPL document "Specification of the Bluetooth System", Version 1.0B (December 1, 1999), 1-1082, which appears to be the same as an NPL document filed October 28, 2002. As a result, the NPL document filed May 14, 2007 has been crossed out. If the NPL document filed

May 14, 2007 is different than the NPL document filed October 28, 2002, applicant needs to resubmit the NPL document and **clearly** indicates that the resubmitted NPL document is not the same as the NPL document filed October 28, 2002.

Claim Objections

4. Claims 2-6 are objected to because of the following informalities: "further" in the preamble of claims 2-6 should be deleted because there is nothing being included in the context data or comprised by accessing context data prior to the recitation of claims 2-6.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

7. Claims 8-13 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter, which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Claim 8 recites "wherein the index register is configured to store the first and second index values". Without further clarification, the limitation suggests that the index

register is configured to store both the first and second index values at the same time. The specification only supports the index register storing either the first index value or the second index value at any given time time.

8. Claims 8-13 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 8 recites the limitation "the host processor" in line 3. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

10. Claims 1, 7-13 are rejected under 35 U.S.C. 102(b) as being anticipated by Anderson et al. (USP 5,613,114).

11. As per claim 1, Anderson teaches a method for performing a context switch operation, comprising:

setting an index register [64, FIG. 1] on an address portion [col. 6, lines 30-32] of a state machine [60, 62, 64, 21-23, 31-33, 41-43, 51-53, FIG. 1] in a peripheral system [20, FIG. 1] to a first index value by a host computer [10, FIG. 1], the first index value

indicating a first register [e.g. 21, 31, 41, 51 - FIG. 1] to be accessed;

accessing context data in the first register of the peripheral system based upon first index value [col. 8, lines 7-12];

setting the index register to a second index value by the host computer, the second index value indicating a second register [e.g. 22, 32, 42, 52 - FIG. 1] to be accessed; and

accessing context data in a second register of the peripheral system when the index register is set to the second index value [col. 8, lines 7-12], wherein the first and second registers are collocated with the peripheral system [the registers are collocated in the peripheral system 20, FIG. 1].

12. As per claim 7, Anderson teaches the registers [21-23, 31-33, 41-43, 51-53, FIG. 1] being dedicated to particular contexts - hence the first and second registers not being architected registers.

13. As per claim 8, Anderson teaches a system comprising:

a host computer [10, FIG. 1], the host computer including a microprocessor [12, FIG. 1];

a peripheral system [20, FIG. 1] coupled to the host microprocessor, the peripheral system including a state machine [60, 62, 64, 21-23, 31-33, 41-43, 51-53, FIG. 1] including an index register [64, FIG. 1], the peripheral system further including a first register [e.g. 21, 31, 41, 51 - FIG. 1] and a second register [e.g. 22, 32, 42, 52 - FIG. 1], the first register being associated with a first index value and the second register being associated with a second index value, wherein the first and second

registers are collocated with the peripheral system (see rejection of claim 1 above).

an interface [29, FIG. 1] coupled to the host computer and to the peripheral system, the interface being configured to provide first and second index values from the host computer to the peripheral system; and

a register access circuit [76, 78 - FIG. 2] in the peripheral system, the register access circuit being configured to access context data in the first register when the first index value is provided by the host computer and set by a thread scheduling unit [74, FIG. 2], wherein the index register is configured to stored the first index value or the second index value, the register access circuit being further configured to access context data in the second register when the second index value is provided by the host computer and set by the thread scheduling unit. Note that "when the first index value is provided by the host computer" and "when the second index value is provided by the host computer" are not specific enough to preclude Anderson from teaching such limitation.

14. As per claim 9, see the rejection of claim 7 above.

15. As per claim 10, Anderson teaches the peripheral system including a state machine module that includes an address portion, a control portion, and a data portion (context switching unit inherently comprising address portion, control portion and data portion), the data portion including the first and second registers (see rejection of claim 8 above).

16. As per claims 11-13, Anderson teaches the peripheral system including a microprocessor [60, 62 - FIG. 1];

the address portion comprising the register access circuit [76, 78 - FIG. 2];

the peripheral system including a plurality of context registers, wherein each of the plurality of context registers is associated with one of a plurality of index values other than the first and second index values [...23-53, FIG. 1].

Claim Rejections - 35 USC § 103

17. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

18. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

19. Claims 2-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Anderson et al..

20. As per claim 2, Anderson does not teach context data including a device address

for a network device, a class value, a clock offset value and an active member address. Such context data are traditionally associated with communications in a Bluetooth environment.

Anderson in essence teaches reducing or eliminating the need for context save and restore when performing context switch operations - by using register sets, each of which being dedicated to a particular context [col. 4, lines 24-36]. Anderson, however, does not teach a Bluetooth environment.

Since it was known in the art at the time the invention was made that traditional context switch operations in a Bluetooth environment require substantial context save and restore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate registers, each of which being dedicated to a particular context (as is taught by Anderson) in a Bluetooth environment - in order to reduce and/or eliminate context save and restore when performing context switch operations in such environment (hence context data in such environment including a device address for a network device, a class value, a clock offset value and an active member address).

21. As per claims 3-6, Anderson teaches each register being dedicated to a thread, hence teaches accessing context data comprising receiving by the peripheral system an address value that identifies an address within the register, control input identifying read/write functions, and data value to write the data value to the register for a write function, or to provide the contents of the register to the host computer for a read function - as read/write threads are known to include address, read/write functions and

data value for read/write functions.

22. Claims 1-13 rejected under 35 U.S.C. 103(a) as being unpatentable over Maupin et al. (USP 6,154,832).

23. As per claim 1, Maupin teaches a method for performing a context switch operation, comprising:

setting an index register [42, FIG. 2] on a state machine [12, 40, 42, 44 - FIG. 2; a processor normally includes state machines and control logics] in a peripheral system [embedded controller 10, FIG. 1] to a first index value by an execution core [40, FIG. 2] of a processor [12, FIG. 2], the first index value indicating a first register to be accessed [a first one of 46A-46H, FIG. 2; col. 6, lines 20-29];

accessing context data in the first register of the peripheral system based upon first index value [col. 6, lines 20-29];

setting the index register to a second index value by the execution core, the second index value indicating a second register to be accessed [a second one of 46A-46H, FIG. 2; col. 6, lines 20-29]; and

accessing context data in a second register of the peripheral system when the index register is set to the second index value [FIG. 5; col. 7, line 63-col. 8, line 8], wherein the first and second registers are collocated with the peripheral system [the registers are collocated on embedded controller 10, FIG. 1].

Maupin further teaches the index register being used to select a register [col. 6, lines 20-29], hence teaches the index register being an address portion (selection of a register implicitly requiring an address) of the state machine (the index register being

considered as part of the state machine).

I. As a first ground of rejection, Maupin also teaches the peripheral system being coupled to an interrupt source [FIG. 1], but does not teach the interrupt source being a host computer. Since it was known in the art at the time the invention was made for an interrupt source of an embedded controller (the peripheral system) to be a host computer in order to allow the host computer to request service from the embedded controller, it would have been obvious to one of ordinary skill in the art at the time the invention was made for the interrupt source of the peripheral system to be a host computer in order to allow the host computer to request service from the peripheral system.

Since a host computer is normally considered to include a peripheral system, and since Maupin teaches the execution core [40, FIG. 2] of the peripheral system setting the index register to an index value, Maupin teaches a host computer setting the index register to an index value (note that the claim requires nothing more than a host computer setting an index register to an index value, and Maupin teaches a host computer setting the index register because the host computer includes the peripheral system).

II. As an alternate ground of rejection and in light of the specification, Maupin essentially discloses the claimed invention except for setting the index register being provided by one entity and except for the state machine being provided by a different entity. It would have been obvious to one having ordinary skill in the art at the time the invention was made to implement the setting of the index register and the state machine

as two different entities (by implementing the setting of the index register as an entity external to processor 12), since it has been held that constructing a formerly integral structure in various elements involves only routine skill in the art. Nerwin v. Erlichman, 168 USPQ 177, 179.

24. As per claim 2, Maupin does not teach context data including a device address for a network device, a class value, a clock offset value and an active member address. Such context data are traditionally associated with communications in a Bluetooth environment.

Maupin in essence teaches reducing or eliminating the need for context save and restore when performing context switch operations - by using register sets, each of which being dedicated to a particular context [col. 4, lines 24-36]. Maupin, however, does not teach a Bluetooth environment.

Since it was known in the art at the time the invention was made that traditional context switch operations in a Bluetooth environment require substantial context save and restore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate registers, each of which being dedicated to a particular context (as is taught by Maupin) in a Bluetooth environment - in order to reduce and/or eliminate context save and restore when performing context switch operations in such environment (hence context data in such environment including a device address for a network device, a class value, a clock offset value and an active member address).

25. As per claims 3-6, Maupin teaches each register being dedicated to a task

corresponding to an interrupt source [col. 4, lines 24-28], hence teaches accessing context data comprising receiving by the peripheral system an address value that identifies an address within the register, control input identifying read/write functions, and data value to write the data value to the register for a write function, or to provide the contents of the register to the interrupt source for a read function - as read/write interrupts are known to include address, read/write functions and data value for read/write functions.

26. As per claim 7, Maupin teaches the registers [46A-46H, FIG. 2] being dedicated to particular contexts - hence the first and second registers not being architected registers.

27. As per claim 8, Maupin teaches a system [FIG. 1] comprising:

a peripheral system [10, FIG. 1] coupled to an interrupt source, the peripheral system including a state machine [12, 40, 42, 44 - FIG. 2; a processor normally includes state machines and control logics] including an index register [42, FIG. 2], the peripheral system further including a first register [a first one of 46A-46H, FIG. 2; col. 6, lines 20-29] and a second register [a second one of 46A-46H, FIG. 2; col. 6, lines 20-29], the first register being associated with a first index value and the second register being associated with a second index value, wherein the first and second registers are collocated with the peripheral system [col. 6, lines 20-29];

an interface [14, FIG. 1] coupled to the interrupt source and to the peripheral system, the interface being configured to provide first and second index values from the interrupt source to the peripheral system [col. 4, lines 24-28]; and

a register access circuit [40, 42, FIG. 2] in the peripheral system, the register access circuit being configured to access context data in the first register when the first index value is provided by the interrupt source and set by the execution core [40, FIG. 2], wherein the index register is configured to stored the first index value or the second index value, the register access circuit being further configured to access context data in the second register when the second index value is provided by the interrupt source and set by the execution core [col. 6, lines 20-29]. Note that "when the first index value is provided by the host computer" and "when the second index value is provided by the host computer" are not specific enough to preclude Maupin from teaching such limitation.

Maupin, therefore teaches the invention except for the external interrupt source being a host computer including a microprocessor. Since it was known in the art at the time the invention was made for an interrupt source of an embedded controller to be a host computer (that inherently includes a microprocessor) in order to allow the host computer to request service from the embedded controller, it would have been obvious to one of ordinary skill in the art at the time the invention was made for the interrupt source of the peripheral system to be a host computer in order to allow the host computer to request service from the peripheral system.

28. As per claims 9-13, Maupin teaches the registers [46A-46H, FIG. 2] being dedicated to particular contexts - hence the first and second registers not being architected registers;

the peripheral system including a state machine module [40, 42, 44, FIG. 2] that

includes an address portion, a control portion, and a data portion (execution core 40 inherently comprising address portion, control portion and data portion), the data portion including the first and second registers [46A-46H included in register file 44, FIG. 2];

the peripheral system including a microprocessor [12, FIG. 1];

the address portion comprising the register access circuit [40, 42, FIG. 2];

the peripheral system including a plurality of context registers, wherein each of the plurality of context registers is associated with one of a plurality of index values other than the first and second index values [8 register sets 46A-46H corresponding to 8 index values].

Double Patenting

29. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and In *re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

30. Claims 1-13 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1, 4-5 of copending Application No. 11/314,036 in view of Maupin.

As per claims 1, 8, 13, claims 1, 5 of the copending application claim all the limitations of the claims except for a context index register for setting the index values. Maupin teaches a context index register for setting a value identifying a new context in a context switch operation. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use a context index register, as is taught by Maupin, in order to identify a new context in a context switch operation.

As per claims 2-6, claim 5 of the copending application claims a Bluetooth network and communications in a Bluetooth network, hence the context data of claim 2, and accessing the context data of claims 3-6.

As per claims 7, 9, claim 4 of the copending application claims non-architected registers.

As per claims 10-12, claim 5 of the copending application claims a host controller, hence a state machine, a microprocessor and a register access circuit in the host controller.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Response to Arguments

31. Applicant's arguments with respect to the pending claims have been considered

but are moot in view of the new ground(s) of rejection.

Conclusion

32. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tanh Q. Nguyen whose telephone number is 571-272-4154. The examiner can normally be reached on M-F 9:30AM-7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim Huynh can be reached on 571-272-4147. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

TANH Q NGUYEN
PRIMARY EXAMINER
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TQN
July 19, 2007